~~said instruction decoder decodes a first instruction among said plurality of~~ instructions and outputs a first control signal in a first period;

said instruction execution unit executes the operation designated by said first instruction in accordance with said first control signal in a second period succeeding to said first period;

said instruction decoder outputs a second control signal by decoding a second instruction of which operation is executed under a predetermined condition among said plurality of instructions in a third period; and

said instruction execution unit [judges] determines whether or not said predetermined condition is satisfied in a fourth period and executes the operation designated by said second instruction in response to a result of the [judgement in a] determination, said fourth period [which is] being started after elapsing [the] a same time ~~as said second period or longer from [the]~~ an ending of ~~said third period.~~

5. (Amended) A data processing device according to Claim 1, wherein

the instruction execution unit [judges] determines whether or not the predetermined condition is satisfied in a fifth period included in said fourth period and executes the operation designated by said second instruction in a sixth period when said predetermined condition is satisfied, said [in a] sixth period [which is] being included in said fourth period and [starts] starting after elapsing the same time as said second period or longer from [the] an ending of said fifth period.

14. (Amended) A data processing device comprising:

an instruction decoder which sequentially decodes a plurality of instructions described in a program sequence and outputs a control signal corresponding to each instruction, and

an instruction execution unit which executes operations designated by the plurality of instructions in accordance with the control signals [outputted] output from said instruction decoder, wherein

when one of said plurality of instructions is a conditional instruction for designating an operation to be executed under a condition, said instruction decoder outputs a first control signal by decoding said conditional instruction;

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said instruction execution unit includes a first register for [holding said first control signal outputted from said instruction decoder, a second register for holding a first description indicating a condition under which an operation designated by the conditional instruction is executed and a third register for] holding a [second] first description indicating a [time] timing for starting a [judgement] determination of said condition; and

said instruction execution unit starts to [judge] determine whether or not said condition is satisfied [based on said first description held in said second register] in response to an event that the [time] timing for starting the [judgement] determination of the condition is detected based on said [second] first description held in said [third] first register [and reads said first control signal held in said first register in response to the result of the judgement], and starts to execute the operation designated by said conditional instruction in accordance with said first control signal and a result of the determination.

15. (Amended) A data processing device according to Claim 14, wherein said [second] first description held in said [third] first register can be variably set.

16. (Amended) A data processing device according to Claim 14, further comprising:

a program counter which sequentially counts an address corresponding to each of the plurality of instructions and holds the address, wherein an address value is held in said [third] first register as said [second] first description; and

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said instruction execution unit, detects an event that the address value held in said [third] first register is in agreement with an address of said program counter and starts to [judge] determine whether or not said condition is satisfied in response to the detection.

17. (Amended) A data processing device according to Claim [15] 25, wherein said conditional instruction has a field for designating an operation which designate contents of the operation, a field for designating condition which designates the executing condition of the operation and a field for designating an amount of delay which designate a [time] timing for [judging] determining the execution condition;

said instruction decoder produces said first control signal based on contents described in said field for designating operation, outputs the second description in accordance with the contents described in said field for designating the condition [as said first description] and outputs the contents described in said field for designating the amount of delay;

said [first] second description [outputted] output from said instruction decoder is held in said [second] third register; and

said instruction execution unit writes said [second] first description in said [third] first register in accordance with said field for designating the amount of delay [outputted] output from said instruction decoder.

18. (Amended) A data processing device according to Claim 14, wherein

the instruction execution unit further has a [fourth] second register for holding a [third] second description indicating a [time] timing for starting the operation designated by the instruction; and

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said instruction execution unit detects the [time] timing for starting the operation designated by the instruction, [judges] determines whether or not the condition is satisfied in response to a result of the detection and starts the operation designated by the instruction in response to a result of the [judgement] determination, in accordance with said [third] second description.

19. (Amended) A data processing device according to Claim 18, further comprising:

a program counter for sequentially counting an address corresponding to each of the plurality of instructions and holds the address, wherein

an address value is held in said [third] first register as said [second] first description;

an address value [which is different from said second description] is held in said [fourth] second register as said [third] second description;

said instruction execution unit detects an event that the address value held in said [third] first register is in agreement with an address of said program counter, starts to [judge] determine whether or not the condition is satisfied in response to the detection, detects an event that the address value held in said [fourth] second register is in agreement with the address of said program counter and starts to execute the operation designated by said instruction in response to the detection.

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20. (Amended) A data processing device according to Claim 18, wherein

said conditional instruction has a field for designating an operation which designate contents of the operation, a field for designating a condition for designating an execution condition of the operation, a field for designating an amount of a first delay which designates a [time] timing for [judging] determining the execution condition and a field for designating an amount of a second delay which designates a [time] timing for starting the execution of the operation;

said instruction decoder produces said first control signal based on the contents described in said field for designating an operation, outputs the second description in accordance with the contents described in said field for designating a condition [as said first description], and outputs the contents described in said field for designating an amount of said first delay and said field for designating an amount of said second delay, the second description output from said instruction decoder is held in said second register; [and]

said instruction execution unit writes said [second] first description in said [third] first register in accordance with the contents described in said field for designating the amount of said first delay [outputted] output from said instruction decoder and further writes said [third] second description in said [fourth] second register in accordance with the contents described in said field for designating the amount of said second delay [outputted] output from said instruction decoder; and

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said instruction execution unit further includes a third register for holding said first control signal output from said instruction decoder and a fourth register for holding a third description indicating the condition, said instruction execution unit performing the determination based on the third description held in said fourth register, reading the first control signal from said third register in response to the result of the determination, and executing the operation in accordance with the first control signal read from said third register.

--21. (New) A data processing device comprising:

an instruction decoder decoding a condition instruction to output a control signal, said condition instruction specifying an operation to be executed under a condition and including a field specifying a timing of starting a determination whether the condition is satisfied; and

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an instruction execution unit starting a determination of the condition on the basis of the field of said condition instruction and executing the operation under a result of the determination.

22. (New) The data processing device according to claim 21, further comprising:

a program counter for calculating and outputting an address specifying an instruction to be fetched, wherein

said instruction execution unit includes a register into which a program counter value is written in accordance with the field of said condition instruction and starts the determination when detecting a coincidence of the program counter value held in said register with an address of said program counter.

23. (New) The data processing device according to claim 22, wherein

said condition instruction includes another field specifying a timing of starting the operation, said instruction execution unit including another register into which a program counter value is written in accordance with the other field of the condition instruction and starting to execute the operation when detecting a coincidence of the program counter value held in the other register with an address of said program counter.

24. (New) The data processing device according to claim 21, wherein

said condition instruction includes another field specifying a timing of starting the operation, said instruction execution unit starting to execute the operation on the basis of the other field of the condition instruction.